

In the Claims:

1.-6. (Canceled)

7. (Currently Amended) A memory cell structure for a memory cell array comprised of a plurality of said memory cells arranged in rows and columns, eolumns; said memory cell structure comprising:

at least two deep trench structures formed in a semiconductor substrate, and along one of said rows, each of said deep trench structures comprising a deep trench defined in said semiconductor substrate, said deep trench having first and second sidewalls extending along a bottom region, a middle region, and an upper region, a dielectric film extending along said first and second sidewalls of said bottom region of said deep trench, a first trench-collar portion extending along said first sidewalls of said middle region and a second trench collar portion extending along said second sidewalls of both said middle and upper regions; at least one of said deep trench structures being in electrical contact with a buried strap region formed in said substrate that adjoins said at least one deep trench structure; and

at least two [[one]] isolation trenches trench adjoining said two deep trench structures, each of said [[one]] isolation trenches extending across said memory cell array trench being defined using a mask comprised of a lines and spaces pattern such that at least one active area is defined by said at least two isolation trenches trench and by said at least two deep trenches, said active area including said buried strap region, each of said lines and said spaces extending across said memory cell array; and

polysilicon filling said bottom and middle regions of said deep trenches.

8. (Original) The memory cell of claim 7 wherein said at least two deep trench structures are separated by a distance $3F$, where F is a minimum feature size.

9. (Currently Amended) The memory cell of claim 7 wherein [[said]] at least an upper portion of said polysilicon filling said middle region is doped polysilicon and further comprising: one deep trench structure comprises:

a trench top oxide formed atop said doped polysilicon; a deep trench formed within a semiconductor substrate;

a gate dielectric layer formed along said first sidewalls of said upper region of said deep trench; a buried plate region adjoining a bottom region of said at least one deep trench within said semiconductor substrate;

a buried strap region in said semiconductor substrate adjoining said first sidewalls, adjacent said doped polysilicon and below said trench top oxide, a dielectric film formed along sidewalls of the deep trench, an upper region of a portion of said dielectric film being removed such that a trench collar is formed along a middle portion of a side of said deep trench, said portion of said dielectric film being defined by a patterned masking layer such that a further portion of said dielectric film is covered by said masking layer and said portion of said dielectric film is exposed;

said deep trench being at least partly filled with doped polysilicon, the dopants in the polysilicon diffusing through said side of said deep trench into an adjoining region of said semiconductor substrate to form said buried strap region along said side of said deep trench.

10. (Currently Amended) The memory cell of claim 9 wherein openings in said masking layer have a pitch equal to twice a minimum feature size in said memory cell, said openings in said masking layer exposing a common region of said dielectric film in each of said plurality of said memory cells, said buried strap region of each of said plurality of said memory cells adjoining a same side of the deep trenches.

11. (Currently Amended) The memory cell of claim 9 wherein openings in said masking layer have a pitch equal to four times that of a minimum feature size of said memory cell, said openings in said masking layer exposing opposing regions of said dielectric film in adjacent ones of said plurality of said memory cells, said buried strap region of said adjacent ones of said plurality of said memory cells adjoining opposite sides of its deep trenches.

12. (Currently Amended) The memory cell of claim 9 further comprising:

a trench top oxide layer formed atop said doped polysilicon in said at least one deep trench;

a gate dielectric layer formed on said side of said deep trench;

said deep trench being filled with a further polysilicon layer atop said trench top oxide layer;

a doped region formed in a top surface of the semiconductor substrate adjacent to said gate dielectric layer;

a contact region to said further polysilicon layer that connects said further polysilicon layer to a word line; and

another contact region to said doped region that connects said doped region to a bit line.

13.-44. (Canceled)

45. (New) The memory cell structure of claim 7 wherein said bottom region of said deep trenches are formed in a heavily doped or buried plate region of said semiconductor substrate such that said buried plate region, said dielectric layer covering said sidewalls of said bottom region of said deep trench and said polysilicon filling said bottom region of said deep trenches comprise the capacitor first plate, the capacitor dielectric and the capacitor second plate of a memory cell capacitor respectively.

46. (New) The memory cell structure of claim 45 further comprising:

- a trench tap oxide formed atop said polysilicon that fills said middle region of said deep trench;
- a further polysilicon layer formed atop said trench top oxide;
- a doped region formed in a top surface of the semiconductor substrate adjacent to said deep trench;
- a contact region to said further polysilicon layer that connects said further polysilicon layer to a word line;
- another contact region to said doped region that connects said doped region to a bit line;
- and
- a transistor having first and second source/drain connections and a gate connection, said gate connection connected to said further polysilicon layer and said word line, one of said first and second source/drain connections connected to said doped region and said bit line and the other one of said first and second source/drain electrically connected to said polysilicon that fills

said bottom region of said deep trench that comprises said second plate of a memory cell capacitor.

47. (New) the memory cell structures of claim 45 further comprising a transistor having first and second source/drain connections and a gate connection, said gate connection connected to a word line, one of said first and second source/drain connections connected to a bit line and the other one of said first and second source/drain connections electrically connected to said polysilicon filling said bottom region of said deep trench that comprises said second plate of a memory cell capacitor.

48. (New) The memory cell structure of claim 46 wherein said doped region is the first source/drain, said buried strap is the second source/drain, and said further polysilicon is the gate of a vertical transistor.

49. (New) The memory cell of claim 46 wherein said at least two deep trench structures are separated by a distance $3F$, where F is a minimum feature size.

50. (New) The memory cell of claim 47 wherein said at least two deep trench structures are separated by a distance $3F$, where F is a minimum feature size.

51. (New) The memory cell of claim 48 wherein said at least two deep trench structures are separated by a distance $3F$, where F is a minimum feature size.